

REMARKS

Applicants' representative extends thanks to Examiner Koyama for the courtesy of a telephone interview on February 6, 2006. In the interview, applicants' representative discussed the prior art of record and identified features recited in the pending claims that Applicant believes are not disclosed in the prior art. An agreement of proposed claim amendments was not reached, and the Examiner suggested that Applicant submit their arguments and any desired claim amendments for further review.

By this Preliminary Amendment, applicant amends claims 44, 50, and 51. No new matter has been added, and the amendments are fully supported by the original specification, see for example, page 14 line 14 through page 16 line 12.

Claims 44-47 and 50

During the interview, Applicant noted that a previous Office Action, mailed November 29, 2005, the Examiner rejected Claims 44 and 50 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,805,290 to Ausschnitt ("Ausschnitt") in view of U.S. Patent No. 6,236,448 to Ota ("Ota"). At page 3 of the Office Action, the Examiner acknowledged that Ausschnitt "fails to teach a stage that is shifted in a desired direction relative to the reticle", but asserted that Ota teaches this limitation.

Applicant respectfully submits that neither Ausschnitt nor Ota, neither individually nor in combination, disclose all of the limitations of Claims 44 and 50. Ausschnitt describes a method for determining critical dimension bias, or overlay error, in a substrate formed by a lithographic substrate. (See Ausschnitt Col. 3, lines 1-3). And, as noted by the Examiner, Ausschnitt does not disclose that a second reticle pattern is shifted in a desired direction and Applicant submits that Ota also fails to disclose this limitation. In addition, Applicant respectfully submits that neither Ausschnitt nor Ota, neither individually nor in combination, disclose determining a self referenced wafer stage overlay error map.

At page 3 of the previous Office Action, the Examiner asserts that Ota discloses an alignment system that determines the relative position shift between positions of reticle marks and wafer marks, and that these represent position shift components in the X-direction and Y-direction. The Examiner notes that Ota describes that "then the

reticle stage 5 is minutely moved in an attempt to reduce all of these position shift components to zero (or to values less than a predetermined reference value)." (See Ota col. 12, lines 4-20.)

Thus, unlike Claims 44 and 50 that recite that "the stage has been shifted in a desired direction relative to the reticle", Ota describes attempting to reduce "position shift components to zero" and that "[o]nce the alignment is achieved the exposure operation is started" and that "[d]uring the exposure operation, the alignment operation is continued." (See Ota col. 12 lines 12-18). In contrast to Claims 45 and 50 that recite that the "stage has been shifted in a desired direction", Ota attempts to reduce any shifting to zero.

Applicant respectfully submits that neither Ausschnitt nor Ota, either individually or in combination, disclose all of the limitations of Claims 44 and 50. As noted by the Examiner, Ausschnitt does not describe all of the limitations of Claims 45 and 50, and the addition of Ota does not overcome these deficiencies. Neither Ausschnitt nor Ota recite that alignment attributes interlock after the stage has been shifted in a desired direction relative to the reticle.

Furthermore, both Ausschnitt and Ota teach away from shifting between exposures. As stated by Ausschnitt, "bias and overlay error may be calculated for the X and Y directions by measurement of distances between edges within an array, or between arrays on the same or different levels." (See Ausschnitt Col. 10 lines 5-8). Because Ausschnitt calculates bias and overlay error by measuring the distances between edges of arrays, any "shift" of the array pattern would be considered an error and would make Ausschnitt inoperable. Likewise, Ota describes that "the reticle stage 5 is minutely moved in an attempt to reduce all of these position shift components to zero (or to values less than a predetermined reference value)." (See Ota col. 12, lines 11-13). Thus, Ota wants to reduce any "shift" to zero, so that any "shift" in the relative positions of the reticle and wafer would be eliminated by Ota.

Moreover, neither Ausschnitt nor Ota, either individually or in combination, disclose determining a self referenced wafer stage overlay error map as recited in Claims 44 and 50. Both Ausschnitt and Ota describe techniques for maintaining

alignment during exposures, not determining a self referenced wafer stage overlay error map.

Applicant respectfully submits that Claims 44 and 50 are patentable over Ausschnitt and Ota, both individually or in combination. Thus, Claims 44 and 50 are in condition for allowance. In addition, Claims 45-47 depend from Claim 44, and are also in condition for allowance.

Claims 51-54

In the previous Office Action, the Examiner rejected Claim 51 under 35 U.S.C. § 103 as being unpatentable over Ausschnitt in view of U.S. Patent No. 5,056,921 to Chaney ("Chaney"). By this paper, Applicant has amended Claim 51 to recite determining a self referenced wafer stage overlay error map. Applicant respectfully submits that neither Ausschnitt nor Chaney, neither individually nor in combination, disclose all of the limitations of Claim 51.

As noted above, Ausschnitt describes a method for determining critical dimension bias, or overlay error, in a substrate formed by a lithographic substrate. In the Office Action, the Examiner acknowledged that Ausschnitt "fails to teach determining a stage distortion and yaw error map", but asserted that Chaney teaches this limitation.

Chaney describes that "the invention relates to optical apparatus for measuring deviations in the movement of a machine component during movement thereof along its main movement axis with an interferometric measuring device." (Chaney Col. 1, lines 7-10). This is in contrast to Claim 51, that recites exposing a reticle pattern that "is shifted in a desired direction" and "thereby creating an interlocking row or column of completed attributes" and that "positional offsets" of the "completed attributes determine a self referenced wafer stage error map." As described above, Ausschnitt also does not describe shifting in a desired direction between exposures nor determining a self referenced wafer stage error map. Thus, Applicant respectfully submits that Claim 51 is patentable over Ausschnitt and Chaney, both individually and in combination.

Furthermore, there would be no motivation to combine Ausschnitt and Chaney. Ausschnitt wants to prevent movement between exposures while Chaney wants to

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**Telephone Interview Summary, Preliminary Amendment
and Accompanying RCE**


measure deviations in the movement of a machine during movement along an axis. Even if Ausschnitt could be combined with Chaney the combination would be inoperable because Ausschnitt wants to eliminate movement while Chaney wants to measure deviations during movement.

Applicant respectfully submits that Claim 51 is patentable over Ausschnitt and Chaney, both individually or in combination. Thus, Claim 51 is in condition for allowance. In addition, Claims 52-54 depend from Claim 51, and are also in condition for allowance.

Conclusion

Applicant respectfully submits that all the pending claims in the application, Claims 44-47 and 50-54, are in condition for allowance. Reconsideration and further examination of the application are requested. A Notice of Allowance is solicited.

Respectfully submitted,
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